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10/601,816	06/23/2003	Heyun Howard Liu	TI-35745	7897

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EXAMINER	
RHU, KRIS M	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/601,816	LIU, HEYUN HOWARD	
	Examiner	Art Unit	
	KRIS RHU	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 36 and 38 are objected to because of the following issues:

a. Claim 36 recites, “the output FIFO generates a stop read signal to the memory array responsive to its contents storing a number of output data words exceeding a second threshold that is higher than the first threshold”. If the second threshold is reached, however, no more reads will be allowed. For the number of output data words stored in the output FIFO to be reduced, there must be reads from the output FIFO. Thus, the claim will be interpreted as the output FIFO generating a stop write signal to the memory array responsive to its contents storing a number of output data words exceeding a second threshold.

b. The term "jumbo packet" in claim 38 is a relative term which renders the claim indefinite. The term "jumbo packet" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US 5,901,100) in view of Dobson (US 5,717,870) and Yeom et al. (US 6,282,203 B1.

Referring to claim 23, Taylor teaches a method of managing the communications of data words arranged in packets; receiving a sequence of input data words at input terminals of the memory circuit **(Data IN 16, Figure 1)**; receiving read strobe signals **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4)**; and sequentially presenting the first and second output data words at output terminals of the memory circuit **(Data OUT 50, Figure 1; "a first-in, first-out ('FIFO') memory device 10 is shown", Column 3, Lines 66-67)**.

Taylor does not appear to teach each packet of data words including a start-of-packet indicator and an end-of-packet indicator; responsive to receiving a first input data word and a second input data word, writing the first and second input data words into a memory array of the memory circuit in a single write cycle; responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet; and responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle.

Dobson teaches responsive to receiving a first input data word and a second input data word, writing the first and second input data words into a memory array of the memory circuit in a single write cycle **(Serial to Parallel Converter 18, Figure 1; Note the RX FIFO 19 can hold 4 words)**; and responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle **(Parallel to Serial Converter 8, Figure 1)**.

Taylor and Dobson are analogous arts because they both teach buffering.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Taylor and Dobson before him or her, to modify Taylor to include responsive to receiving a first input data word and a second input data word, writing the first and second input data words into a memory array of the memory circuit in a single write cycle; and responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle, as taught by Dobson, because it would merely involve utilizing a known concept of deserializing received data before writing into of a FIFO and serializing data before reading out of a FIFO.

Therefore, it would have been obvious to combine Dobson with Taylor to obtain the invention as specified in the instant claim.

Yeom teaches each packet of data words including a start-of-packet indicator and an end-of-packet indicator **("The hardware router 21 checks the**

ninth bits and detects the start and end of the packet", Column 3, Lines 40-41), and responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet **("Once the last byte of the packet is written to the transmitting buffer 220, the node 200 sends a packet ready signal, PKTRDY, to the hardware router 21", Column 3, Lines 41-44)**.

Taylor/Dobson and Yeom are analogous arts because they both teach buffering.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Taylor/Dobson and Yeom before him or her, to modify Taylor/Dobson to include each packet of data words including a start-of-packet indicator and an end-of-packet indicator, and responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet because it would merely involve utilizing a known concept of detecting the start and end of a packet and utilizing a packet ready signal as an enabling signal for enabling the output of data words once both the start and end of the packet has been detected.

Therefore, it would have been obvious to combine Yeom with Taylor/Dobson to obtain the invention as specified in the instant claim.

As to claim 24, Taylor/Dobson/Yeom teaches the method of claim 23, further comprising: enabling the output of data words corresponding to the

packet, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor; Note the clearing of the empty flag indicates that at least the start of one packet has been written into the FIFO memory, enabling reading from the FIFO memory)**.

As to claim 25, Taylor/Dobson/Yeom teaches the method of claim 23, further comprising: incrementing a count of the number of packets stored in the memory array responsive to detecting the writing of an end-of-packet indicator **(Write Row Counter, Column 6, Taylor)**.

As to claim 26, Taylor/Dobson/Yeom teaches the method of claim 25, further comprising: disabling the outputting of output data words, responsive to the outputting of an end-of- packet indication for a packet and to the count indicating that no additional packets are stored **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

As to claim 27, Taylor/Dobson/Yeom teaches the method of claim 26, wherein the disabling step comprises: controlling an output register to disable the presenting of output data words at the output terminals **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

4. Claims 28-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna et al. (US 6,252,880 B1) in view of Taylor and Dobson.

Referring to claim 28, Hanna teaches a network node for controlling the transmission and receipt of packet- based data over a communications facility, comprising: a system interface **(Network Port 12, Figure 1)** for receiving transmit data from a system **(Network Station 14, Figure 1)** and for outputting processed received signals to the system; a transmit FIFO buffer **(Transmit FIFO Buffer 26, Figure 1)**, for buffering transmit data received at the system interface; a transceiver **(Network Port 12, Figure 1)**, for driving the communications facility with transmitted signals corresponding to the transmit data, and for receiving signals from the communications facility; and a receive FIFO buffer **(Receive FIFO Buffer 24, Figure 1)**, for buffering the received signals.

Hanna does not appear to teach each of the transmit and receive FIFO buffers comprising: a memory array; a clock terminal for receiving a clock signal; a write enable terminal for receiving a write enable signal; inputs for receiving input data words; a read enable terminal for receiving a read enable signal; outputs for presenting output data words of the same word width as that of the input data words; a write buffer, coupled to the inputs and to the array of memory cells, for receiving a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, and for writing the first and second input data words to the memory array in a single write cycle; read circuitry, for requesting a read of the memory array responsive to receiving first and second read enable signals at the read

enable terminal; and a read buffer, for receiving first and second output data words from the memory array responsive to the request of the read of the memory array, and for presenting the first and second output data words in sequence to the outputs.

Taylor, however, teaches each of the transmit and receive FIFO buffers comprising: a memory array **("The memory device 10 comprises, in pertinent part, a primary DRAM memory array", Column 4, Lines 1-2)**; a clock terminal **(Write Clock 36 and Read Clock 38, Figure 1)** for receiving a clock signal; a write enable terminal for receiving a write enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4)**; inputs for receiving input data words **(Data IN 16, Figure 1)**; a read enable terminal for receiving a read enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4)**; outputs for presenting output data words of the same word width as that of the input data words **(Data OUT 50, Figure 1; "The inputs and outputs 16, 50 are word-wide", Column 5, Line 29)**; a write buffer **(Input Buffer 22, Figure 1)**, coupled to the inputs and to the array of memory cells, for receiving a sequence **(Note memory device 10 is a FIFO)** of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal; read circuitry **(I/O and Control 42, Figure 1)**, for requesting a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and a read buffer **("the FIFO memory device 10 may**

also incorporate:…an output or multiple output buffers to enhance FIFO memory device 10 performance", Column 4, Line 65 to Column 5, Line 6, Taylor), for receiving first and second output data words from the memory array responsive to the request of the read of the memory array, and for presenting the first and second output data words in sequence **(Note memory device 10 is a FIFO)** to the outputs.

Hanna and Taylor are analogous arts because they both teach FIFOs.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Hanna and Taylor before him or her, to modify Hanna to include each of the transmit and receive FIFO buffers comprising: a memory array; a clock terminal for receiving a clock signal; a write enable terminal for receiving a write enable signal; inputs for receiving input data words; a read enable terminal for receiving a read enable signal; outputs for presenting output data words of the same word width as that of the input data words; a write buffer, coupled to the inputs and to the array of memory cells, for receiving a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal; read circuitry, for requesting a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and a read buffer, for receiving first and second output data words from the memory array responsive to the request of the read of the memory array, and for presenting the first and second output data words in sequence to the outputs, as taught by

Taylor, because it would merely involve substituting the FIFOs taught in Taylor for the FIFOs taught in Hanna.

Therefore, it would have been obvious to combine Taylor with Hanna to obtain the invention as specified in the instant claim.

Dobson teaches writing the first and second input data words to the memory array in a single write cycle **(Serial to Parallel Converter 18, Figure 1; Note the RX FIFO 19 can hold 4 words)**.

Hanna/Taylor and Dobson are analogous arts because they both teach FIFOs.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Hanna/Taylor and Dobson before him or her, to modify Hanna/Taylor to include writing the first and second input data words to the memory array in a single write cycle, as taught by Dobson, because it would merely involve utilizing a known concept of deserializing received data before writing to the receive FIFO.

Therefore, it would have been obvious to combine Dobson with Hanna/Taylor to obtain the invention as specified in the instant claim.

As to claim 29, Hanna/Taylor/Dobson teaches the network node of claim 28, wherein the transceiver comprises: a serializer **(Parallel to Serial Converter 8, Figure 1, Dobson)**, for serializing the transmit data; a line driver, for driving the communications facility with serial signals from the serializer **(Serial Data line 9, Figure 1, Dobson)**; a receiver **(the input port receiving from serial**

data line 17, Figure 1, Dobson), for receiving serial signals from the communications facility; and a deserializer **(Serial to Parallel Converter 18, Figure 1, Dobson)**, for deserializing the signals received by the receiver.

As to claim 30, Hanna/Taylor/Dobson teaches the network node of claim 28, further comprising: a transmit media access control function **(MAC layer transmitter 22, Figure 1, Hanna)**, for processing the transmit data buffered by the transmit FIFO buffer; and a receive media access control function **(MAC layer receiver 20, Figure 1, Hanna)**, for processing the received signals and applying the processed received signals to the receive FIFO buffer.

As to claim 31, Hanna/Taylor/Dobson teaches the network node of claim 28, wherein the write buffer in each of the transmit and receive FIFO buffers comprises: a plurality of buffer storage locations arranged in rows and columns **("the FIFO memory device 10 memory is organized as Y rows by X columns and the columns are word-wide as well", Column 5, Lines 30-32, Hanna; Note though Hanna teaches the memory array of the FIFO being organized in two dimensions, it would have been obvious to have the buffers of a FIFO organized in two dimensions because it would merely involve applying a known concept of organizing a memory in two dimensions to another type of memory, buffers)**, including first and second columns of buffer storage locations having storage locations in first and second rows; and sequential logic, for controlling the write buffer to store a first input data word in a buffer storage location at the first row and the first column, and to store a second

input data word in a buffer storage location at the second row and the first column **(Note it is obvious to store the words in sequence. After all, a FIFO is being used which is a first-in-first-out buffer)**, and to then forward the first and second input data words to the memory array in an internal write cycle **("the FIFO memory device 10 may also incorporate: an internal clock", Column 4, Lines 65-67, Taylor)**.

As to claim 32, Hanna/Taylor/Dobson teaches the network node of claim 31, wherein the write buffer in each of the transmit and receive FIFO buffers comprises: a clock input **(Write Clock 36 and Read Clock 38, Figure 1, Taylor)** for receiving a periodic clock signal; and clock circuitry **("the FIFO memory device 10 may also incorporate: an internal clock", Column 4, Lines 65-67, Taylor)**, for assigning alternating cycles of the periodic clock signal as internal write and internal read cycles; wherein the sequential logic also controls the write buffer to then store a third input data word in a buffer storage location of the second column responsive to the inputs receiving the third input data word prior to an internal write cycle **("the FIFO memory device 10 memory is organized as Y rows by X columns and the columns are word-wide as well", Column 5, Lines 30-32, Hanna; Note though Hanna teaches the memory array of the FIFO being organized in two dimensions, it would have been obvious to have the buffers of a FIFO organized in two dimensions because it would merely involve applying a known concept of organizing a memory in two dimensions to another type of memory, buffers)**.

As to claim 33, Hanna/Taylor/Dobson teaches the network node of claim 28, wherein the read buffer in each of the transmit and receive FIFO buffers comprises: an output width converter **(Parallel to Serial Converter 8, Figure 1, Dobson)**, for converting double-width output data words read from the memory array into a sequence of output data words; and an output FIFO **(Transmit FIFO, Figure 1, Dobson)**, coupled to the output width converter, for buffering the output data words in a first-in-first-out fashion.

As to claim 34, Hanna/Taylor/Dobson teaches the network node of claim 33, wherein the read circuitry further comprises: an output register **("The input buffer 22 may be implemented in several ways (i.e. as a shift register)", Column 5, Lines 50-51, Taylor; Note it would be obvious to implement the pre-output buffer 48 as a shift register as well)** for presenting an output data word received from the output FIFO at the outputs, in combination with a data valid signal **(IBC – indicates the number of valid words in the input buffer, Column 6, Taylor)**, responsive to the read circuitry receiving a read enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4, Taylor)**.

As to claim 35, Hanna/Taylor/Dobson teaches the network node of claim 33, wherein the output FIFO generates a read ready signal responsive to its contents storing a number of output data words exceeding a first threshold **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-**

16, Taylor; Thus, when the empty flag is cleared, the FIFO will be Allowed to read).

As to claim 36, Hanna/Taylor/Dobson teaches the network node of claim 35, wherein the output FIFO generates a stop read signal to the memory array responsive to its contents storing a number of output data words exceeding a second threshold that is higher than the first threshold **("The full flag, therefore, prevents writing while full", Column 2, Lines 22-23, Taylor)**; and wherein the output FIFO generates a start read signal to the memory array responsive to its contents storing a number of output data words below a third threshold that is lower than the first threshold.

Claim Rejections - 35 USC § 103

5. Claims 37-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna/Taylor/Dobson in view of Yeom.

As to claim 37, Hanna/Taylor/Dobson does not appear to teach the network node of claim 28, wherein each packet of data words includes a start-of-packet indicator and an end-of-packet indicator; and wherein each of the transmit and receive FIFO buffers further comprise: packet management logic, for controlling the operation of the memory circuit, the packet management logic for enabling the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator.

Yeom, however, teaches each packet of data words including a start-of-packet indicator and an end-of-packet indicator **("The hardware router 21 checks the ninth bits and detects the start and end of the packet", Column 3, Lines 40-41)** and the transmission of a packet ready signal when the start and end of the packet has been detected **("Once the last byte of the packet is written to the transmitting buffer 220, the node 200 sends a packet ready signal, PKTRDY, to the hardware router 21", Column 3, Lines 41-44)**.

Hanna/Taylor/Dobson and Yeom are analogous arts because they both teach buffering.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Hanna/Taylor/Dobson and Yeom before him or her, to modify Hanna/Taylor/Dobson to include wherein each packet of data words includes a start-of-packet indicator and an end-of-packet indicator; and wherein each of the transmit and receive FIFO buffers further comprise: packet management logic, for controlling the operation of the memory circuit, the packet management logic for enabling the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator because it would merely involve utilizing a known concept of detecting the start and end of a packet and utilizing a packet ready signal as an enabling signal for enabling the output of data words once both the start and end of the packet has been detected.

Therefore, it would have been obvious to combine Yeom with Hanna/Taylor/Dobson to obtain the invention as specified in the instant claim.

As to claim 38, Hanna/Taylor/Dobson teaches the network node of claim 37, wherein the packet management logic is also for enabling the outputting of output data words corresponding to a jumbo packet **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4, Taylor; Note the FIFO can store multiple words. Thus, it can store data packets that are multiple words long)**, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

As to claim 39, Hanna/Taylor/Dobson teaches the network node of claim 37, wherein the packet management logic is also for maintaining a count of the number of packets stored in the memory array **("write row counter" and "read row counter", Column 6 and Column 7, Taylor)**.

As to claim 40, Hanna/Taylor/Dobson teaches the network node of claim 39, wherein the packet management logic is also for disabling the outputting of output data words, responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

As to claim 41, Hanna/Taylor/Dobson teaches the network node of claim 40, wherein the read buffer comprises: an output width converter **(Parallel to**

Serial Converter 8, Figure 1, Dobson), for converting double-width output data words read from the memory array into a sequence of output data words; an output FIFO **(Tx FIFO 7, Figure 1, Dobson)**, coupled to the output width converter, for buffering the output data words in a first-in-first-out fashion; and an output register **("The input buffer 22 may be implemented in several ways (i.e. as a shift register)", Column 5, Lines 50-51, Taylor; Note it would be obvious to implement the pre-output buffer 48 as a shift register as well)** for presenting an output data word received from the output FIFO at the outputs, in combination with a data valid signal **(IBC – indicates the number of valid words in the input buffer, Column 6, Taylor)**, responsive to the read circuitry receiving a read enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4, Taylor)**, and wherein the packet management logic controls the output register to disable the outputting of output data words responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Firoozmand (US 5,488,724) teaches buffers that comprise a transmit FIFO and a receive FIFO.

Firoozmand (US 5,210,749) teaches buffers that comprise a transmit FIFO and a receive FIFO.

Muller et al. (US 6,650,640) teaches packet size indicators.

Davis (US 7,468, 975 B1) teaches transferring jumbo packets

Chow et al. (US 6,839,351) teaches network nodes comprising receive FIFOs.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KRIS RHU whose telephone number is 571-270-1728. The examiner can normally be reached on MTWThF 8:30-6 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KR

/Henry W.H. Tsai/

Supervisory Patent Examiner, Art Unit 2184